

CLAIMS

- 1 1. A method for finding the boundary between words in a stream of data bits, each
2 data bit defining a bit cycle, the method comprising the steps of:
3 defining a high and a low logic level;
4 determining the sequence of bits defining a word;
5 selecting a data signal defining a word boundary;
6 adding the word boundary with the bits defining the word;
7 sending out in serial form the word data bits with the added word boundary;
8 sending out in parallel with the data bits, a bit clock synchronized with the data
9 bits;
10 causing the bit clock to maintain a constant logic level during the sending of the
11 word boundary; and
12 determining the word boundary by sensing the word boundary while the bit clock
13 maintains a constant logic level.
- 1 2. The method of claim 1 wherein the step of selecting the boundary comprises the
2 step of creating logic level transitions at a double bit cycle frequency during a bit cycle,
3 the double bit cycle during a bit cycle defining the word boundary.
- 1 3. The method of claim 1 wherein the step of determining a word boundary com-
2 prises the step of:
3 selecting two added boundary data bits, the data bits having the same bit cycle as
4 the data bits, the boundary data bits selected so that there is a logic level transition at the
5 beginning of the first boundary bit and at the junction of the two added boundary data
6 bits.
- 1 4. The method of claim 1 wherein the clock logic level remains high during a word
2 boundary.

- 1 5. The method of claim 1 wherein the clock logic level remains low during a word
2 boundary.
- 1 6. The method of claim 3 wherein the logic level transition at the junction of the two
2 boundary bits is from low to high.
- 1 7. The method of claim 3 wherein the logic level transition at the junction of the two
2 boundary bits is from high to low.
- 1 8. The method of claim 1 further comprising the steps of placing filler bits before
2 and after the data word and word boundary.
- 1 9. The method of claim 1 wherein the word boundary is placed within the word data
2 bits.
- 1 10. The method of claim 1 wherein the word boundary is placed before the word data
2 bits.
- 1 11. The method of claim 1 wherein the word boundary is placed after the word data
2 bits.
- 1 12. The method of claim 3 further comprising the steps of:
2 loading a parallel data word into a shift register;
3 defining the word boundary as bits sharing the same bit cycle as the word data
4 bits;
5 loading the word boundary bits into the shift register;
6 shifting out the word data bits and the word boundary bits; and
7 loading the next parallel data word and word boundary bits into the shift register.

1 13. The method of claim 1 further comprising the steps of:
2 defining the word boundary as bits sharing the same bit cycle as the word data
3 bits;
4 receiving the serial word data bits and the word boundary bits;
5 receiving the synchronous bit clock;
6 shifting the received word data bits and the word boundary bits, bit by bit, into a
7 shift register using the received synchronous bit clock;
8 detecting when a data word has been shifted into the shift register, and in response
9 indicating the receipt of the word to a computing system; and
10 reading the word by the computing system.

1 14. Apparatus for finding the boundary between words in a stream of data bits, each
2 data bit defining a bit cycle, the apparatus comprising:
3 means for defining a high and a low logic level;
4 means for determining the sequence of bits defining a word;
5 means for selecting a data signal defining a word boundary;
6 means for adding the word boundary with the bits defining the word;
7 means for sending out in serial form the word data bits with the added word
8 boundary;
9 means for sending out in parallel with the data bits, a bit clock synchronized with
10 the data bits;
11 means for causing the bit clock to maintain a constant logic level during the send-
12 ing of the word boundary; and
13 means for determining the word boundary by sensing the word boundary while
14 the bit clock maintains a constant logic level.

1 15. The apparatus of claim 14 wherein the means for selecting the data signal defin-
2 ing a word boundary comprises means for creating logic level transitions at a double bit
3 cycle frequency during a bit cycle, the double bit cycle during a bit cycle defining the
4 word boundary.

- 1 16. The apparatus of claim 14 wherein the means for determining a word boundary
2 comprises:
3 means for selecting two added boundary data bits having the same bit cycle as the
4 data bits, the boundary data bits selected so that there is a logic level transition at the
5 junction of the two added boundary data bits.
- 1 17. The apparatus of claim 14 wherein the clock logic level remains high during a
2 word boundary.
- 1 18. The apparatus of claim 14 wherein the clock logic level remains low during a
2 word boundary.
- 1 19. The apparatus of claim 14 wherein the logic level transition at the junction of the
2 two boundary bits is from low to high.
- 1 20. The apparatus of claim 14 wherein the logic level transition at the junction of the
2 two boundary bits is from high to low.
- 1 21. The apparatus of claim 14 further comprising means for placing filler bits before
2 and after the data word and word boundary.
- 1 22. The apparatus of claim 14 wherein the word boundary is placed within the word
2 data bits.
- 1 23. The apparatus of claim 14 wherein the word boundary is placed before the word
2 data bits.
- 1 24. The apparatus of claim 14 wherein the word boundary is placed after the word
2 data bits.

1 25. The apparatus of claim 17 further comprising:
2 means for loading a parallel data word into a shift register;
3 means for defining the word boundary as bits sharing the same bit cycle as the
4 word data bits;
5 means for loading the word boundary bits into the shift register;
6 means for shifting out the word data bits and the word boundary bits; and
7 means for loading the next parallel data word and word boundary bits into the
8 shift register.

1 26. The apparatus of claim 14 further comprising:
2 means for defining the word boundary as bits sharing the same bit cycle as the
3 word data bits;
4 means for receiving the serial word data bits and the word boundary bits;
5 means for receiving the synchronous bit clock;
6 means for shifting the received word data bits and the word boundary bits, bit by
7 bit, into a shift register using the received synchronous bit clock;
8 means for detecting when a data word has been shifted into the shift register, and
9 in response;
10 means for indicating the receipt of the word to a computing system; and
11 means for reading the word by the computing system.